Amendments to the Claims

Claims 1-43 (Cancelled).

44. (Currently amended) A method of forming a dynamic random access memory (DRAM) comprising:

forming a plurality of conductive lines over a substrate having a memory array area and a peripheral area outward of the memory array area;

forming conductive material over the substrate comprising:

conductive plugs received over substrate node locations over which storage capacitors are to be formed within the memory array area, and

conductive material received over portions of some of the conductive lines within the peripheral area;

forming openings through an insulative material and exposing the conductive plugs within the memory array area and the conductive material within the peripheral area;

forming a storage capacitor electrode layer within the openings; ~~and~~

removing portions of the storage capacitor electrode layer within the memory array area ~~and peripheral area~~ sufficient to form a storage capacitor electrode within the memory ~~array~~ array; and

entirely removing ~~remove~~ the storage capacitor electrode layer and at least some of the conductive material received over the conductive lines ~~from~~ within the peripheral area and outwardly expose conductive portions of conductive lines within the peripheral area.

45. (Original) The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a cell plate layer within the openings.

46. (Original) The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a cell plate layer within the openings, and wherein the removing of the storage capacitor electrode layer comprises doing so in a common masking step.

47. (Original) The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a cell plate layer within the openings, and wherein the removing of the storage capacitor electrode layer comprises doing so in a common etching step.

48. (Original) The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a storage node layer within the openings.

49. (Original) The method of claim 44, wherein the forming of the storage capacitor electrode layer comprises forming a storage node layer within the openings, and wherein the removing of the storage capacitor electrode layer comprises doing so in multiple removing steps.

50. (New) A method of forming a dynamic random access memory (DRAM), comprising:

providing a substrate having conductive lines disposed within a memory array area and having conductive lines disposed within a peripheral area;

forming a plurality of conductive plugs within the memory array area;

forming a first insulative material over the conductive plugs and over the conductive lines disposed within the peripheral area;

forming a first plurality of openings extending through the first insulative material within the memory array area to expose the conductive plugs;

forming a second plurality of openings through the first insulative material to expose a second insulative material comprised by the conductive lines disposed within the peripheral area;

forming a first conductive material within the first and second pluralities of openings; and

entirely removing the first conductive material from within the second plurality of openings and extending the second plurality of openings to expose a second conductive material comprised by the conductive lines disposed within the peripheral area.

51. (New) The method of claim 50 wherein the first and second pluralities of openings are formed simultaneously.

52. (New) The method of claim 50 wherein the first conductive material comprises conductively doped polysilicon.

53. (New) The method of claim 50 further comprising forming a dielectric material over the first conductive material and forming a third conductive material over the dielectric material prior to removing the first conductive material from within the second plurality of openings.

54. (New) The method of claim 50 wherein the second conductive material comprises a silicide.

55. (New) The method of claim 50 wherein the second insulative material comprises silicon nitride.

56. (New) The method of claim 50 further comprising, after extending the second conductive material, forming a contact plug in electrical communication with the second conductive material.

57. (New) The method of claim 50 wherein removing the first conductive material and extending the second plurality of openings utilize a common etch chemistry.

58. (New) The method of claim 57 wherein the etch chemistry comprises NF_3 and HBr.